# GX8563 Real-time clock/calendar

## 1 Features

• Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal

• Century flag

• Clock operating voltage: 1.0 V to 5.5 V at room temperature

• Low backup current; typical 0.25 μA at $V_{DD}$ = 3.0 V and Tamb = 25 ˚C

• 400 kHz two-wire $I^2C$-bus interface (at $V_{DD}$ = 1.8 V to 5.5 V)

• Programmable clock output for peripheral devices (32.768 kHz, 1.024 kHz, 32 Hz, and 1 Hz)

• Alarm and timer functions

• Integrated oscillator capacitor

• Internal Power-On Reset (POR)

• $I^2C$-bus slave address: read A3h and write A2h

• Open-drain interrupt pin

## 2 Applications

• Mobile telephones

• Portable instruments

• Electronic metering

• Battery powered products

## 3 Description

The GX8563 is a CMOS Real-Time Clock (RTC) and calendar optimized for low power consumption. A programmable clock output, interrupt output, and voltage-low detector are also provided. All addresses and data are transferred serially via a two-line bidirectional $I^2C$-bus. Maximum bus speed is 400 kbit/s. The register address is incremented automatically after each written or read data byte.

## Version History

| Version | Date | Description |
|---|---|---|
| V1.0 | 2023/1/31 | Original version |
| V1.1 | 2023/2/4 | Change format |
| V2.0 | 2023/3/4 | Add SOP8 package |
| V2.1 | 2023/4/10 | Change package picture |
| V2.2 | 2023/6/12 | Change application circuit |
| V2.3 | 2023/6/15 | Change application capacitor |
| V2.4 | 2024/8/22 | Add MSL level |
| V2.5 | 2024/12/4 | Update HBM $V_{ESD}$ |
| V2.6 | 2025/4/29 | Update dynamic characteristics |

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# 4 Block Diagram

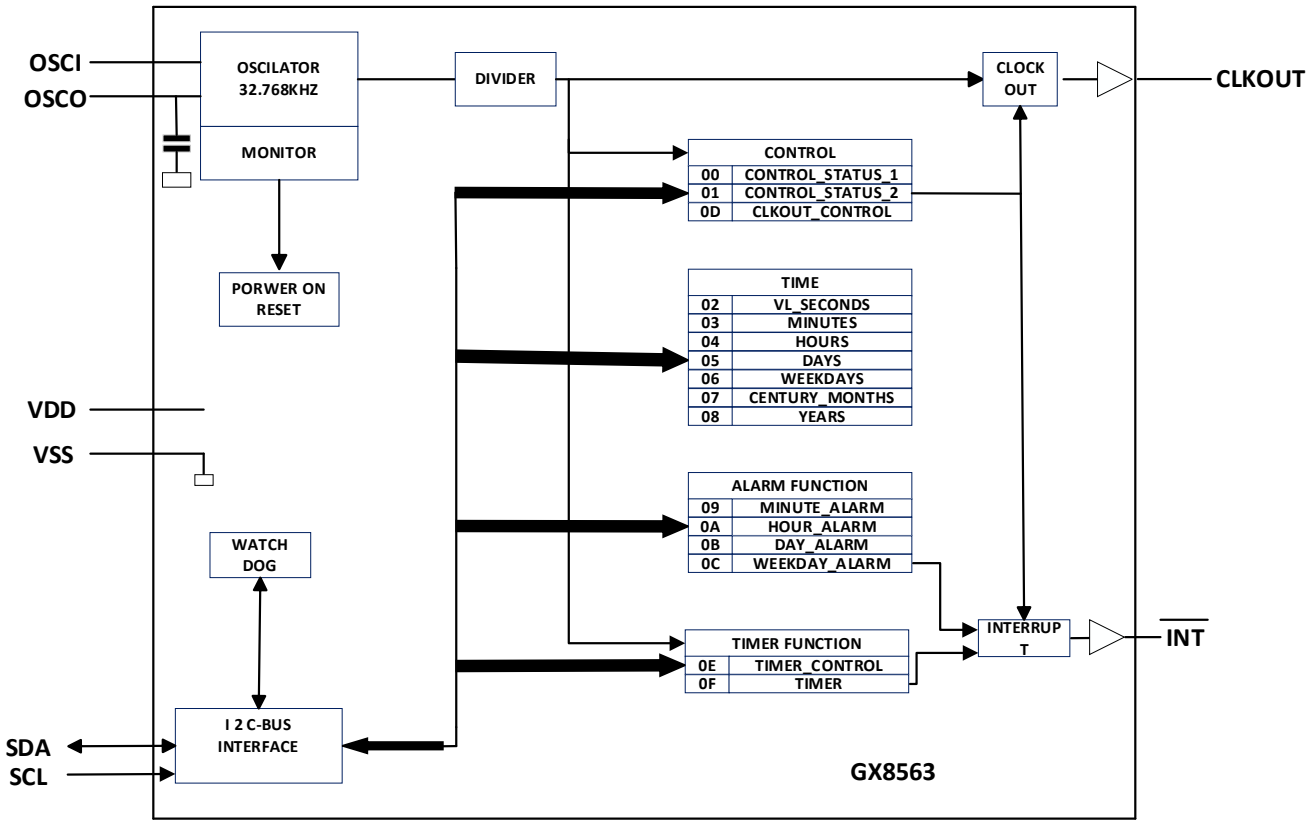



**Figure 1. Block diagram of GX8563**

# 5 Pinning Information

## 5.1 Pinning

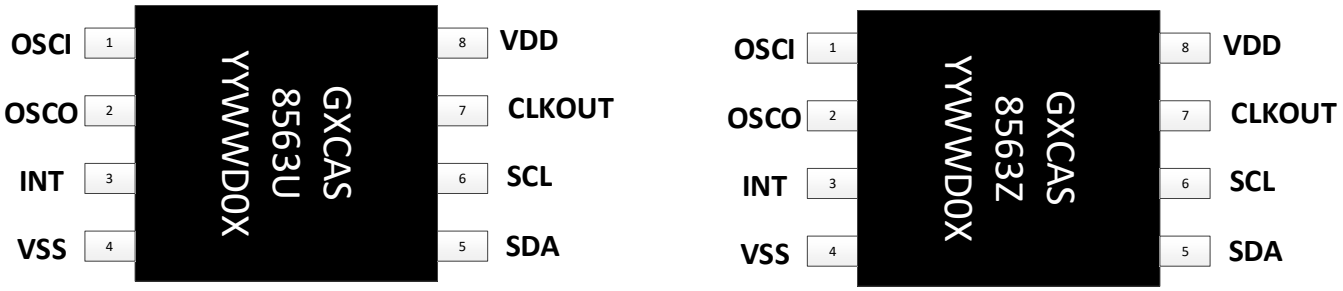



**Figure 2. Pin configuration for GX8563**

## 5.2 Pin Description

**Table 1. Pin description**

| SYMBOL | PIN | | DESCRIPTION |
|---|---|---|---|
| | MSOP8 | SOP8 | |
| OSCI | 1 | 1 | oscillator input |
| OSCO | 2 | 2 | oscillator output |
| INT | 3 | 3 | interrupt output (open-drain; active LOW) |
| $V_{SS}$ | 4 | 4 | ground |
| SDA | 5 | 5 | serial data input and output |
| SCL | 6 | 6 | serial clock input |
| CLKOUT | 7 | 7 | clock output, open-drain |
| $V_{DD}$ | 8 | 8 | supply voltage |
| n.c. | - | | not connected; do not connect and do not use as feed |

[1] The die paddle (exposed pad) is wired to $V_{SS}$ but should not be electrically connected.

# 6 Functional Description

The GX8563 contains sixteen 8-bit registers with an auto-incrementing register address, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calender, a programmable clock output, a timer, an alarm, a voltage-low detector, and a 400 kHz I2C-bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and/or status registers. The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years counters). Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm.

Address 0Dh controls the CLKOUT output frequency. 0Eh and 0Fh are the Timer_control and Timer registers, respectively.

The Seconds, Minutes, Hours, Days, Months, Years as well as the Minute_alarm, Hour_alarm, and Day_alarm registers are all coded in Binary Coded Decimal (BCD) format.

When one of the RTC registers is written or read, the contents of all time counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.

## 6.1 CLKOUT Output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the register CLKOUT_control at address 0Dh. Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz, and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance.

## 6.2 Register Organization

**Table 2. Formatted registers overview**

| ADDRESS | REGISTER NAME | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Control and status registers** | | | | | | | | | |
| 00h | Control_status_1 | TEST1 | N | STOP | N | TESTC | N | N | N |
| 01h | Control_status_2 | N | N | N | TI_TP | AF | TF | AIE | TIE |
| **Time and date registers** | | | | | | | | | |
| 02h | VL_seconds | VL | SECONDS (0 to 59) | | | | | | |
| 03h | Minutes | x | MINUTES (0 to 59) | | | | | | |
| 04h | Hours | x | x | HOURS (0 to 23) | | | | | |
| 05h | Days | x | x | DAYS (1 to 31) | | | | | |
| 06h | Weekdays | x | x | x | x | x | WEEKDAYS (0 to 6) | | |
| 07h | Century_months | C | x | x | MONTHS (1 to 12) | | | | |
| 08h | Years | YEARS (0 to 99) | | | | | | | |
| **Alarm registers** | | | | | | | | | |
| 09h | Minute_alarm | AE_M | MINUTE_ALARM (0 to 59) | | | | | | |
| 0Ah | Hour_alarm | AE_H | x | HOUR_ALARM (0 to 23) | | | | | |
| 0Bh | Day_alarm | AE_D | x | DAY_ALARM (1 to 31) | | | | | |
| 0Ch | Weekday_alarm | AE_W | x | x | x | x | WEEKDAY_ALARM (0 to 6) | | |
| **CLKOUT control register** | | | | | | | | | |
| 0Dh | CLKOUT_control | FE | x | x | x | x | x | FD[1:0] | |
| **Timer registers** | | | | | | | | | |
| 0Eh | Timer_control | TE | x | x | x | x | x | TD[1:0] | |
| 0Fh | Timer | TIMER[7:0] | | | | | | | |

Bit positions labelled as x are not relevant. Bit positions labelled with N should always be written with logic 0; if read they could be either logic 0 or logic 1. After reset, all registers are set according to Table 2.

## 6.3 Control registers

### 6.3.1 Register Control_status_1

**Table 3. Control_status_1 - control and status register 1 (address 00h) bit description**

| BIT | SYMBO | VALUE | DESCRIPTION |
|---|---|---|---|
| 7 | TEST1 | default 0 | normal mode, must be set to logic 0 during normal operations |
| | | 1 | EXT_CLK test mode |
| 6 | N | 0[1] | unused |
| 5 | STOP | default 0 | RTC source clock runs |

| | | | |
|---|---|---|---|
| | | 1 | all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available) |
| 4 | N | 0[1] | unused |
| 3 | TESTC | 0 | Power-On Reset (POR) override facility is disabled; set to logic 0 for normal operation |
| | | default 1 | Power-On Reset (POR) override may be enabled |
| 2 to 0 | N | 000[1] | unused |

[1] Bits labeled as N should always be written with logic 0.

### 6.3.2 Register Control_status_2

**Table 4. Control_status_2 - control and status register 2 (address 01h) bit description**

| BIT | SYMBO | VALUE | DESCRIPTION |
|---|---|---|---|
| 7 to 5 | N | 000[1] | unused |
| 4 | TI_TP | default 0 | INT is active when TF is active (subject to the status of TIE) |
| | | 1 | $\overline{\text{INT}}$ pulses active according to Table 4 (subject to the status of TIE); Remark: note that if AF and AIE are active then $\overline{\text{INT}}$ will be permanently active |
| 3 | AF | default 0 | read: alarm flag inactive |
| | | | write: alarm flag is cleared |
| | | 1 | read: alarm flag active |
| | | | write: alarm flag remains unchanged |
| 2 | TF | default 0 | read: alarm flag inactive |
| | | | write: alarm flag is cleared |
| | | 1 | read: alarm flag active |
| | | | write: alarm flag remains unchanged |
| 1 | AIE | default 0 | alarm interrupt disabled |
| | | 1 | alarm interrupt enabled |
| 0 | TIE | default 0 | timer interrupt disabled |
| | | 1 | timer interrupt enabled |

[1] Bits labeled as N should always be written with logic 0.

### 6.3.2.1 Interrupt output

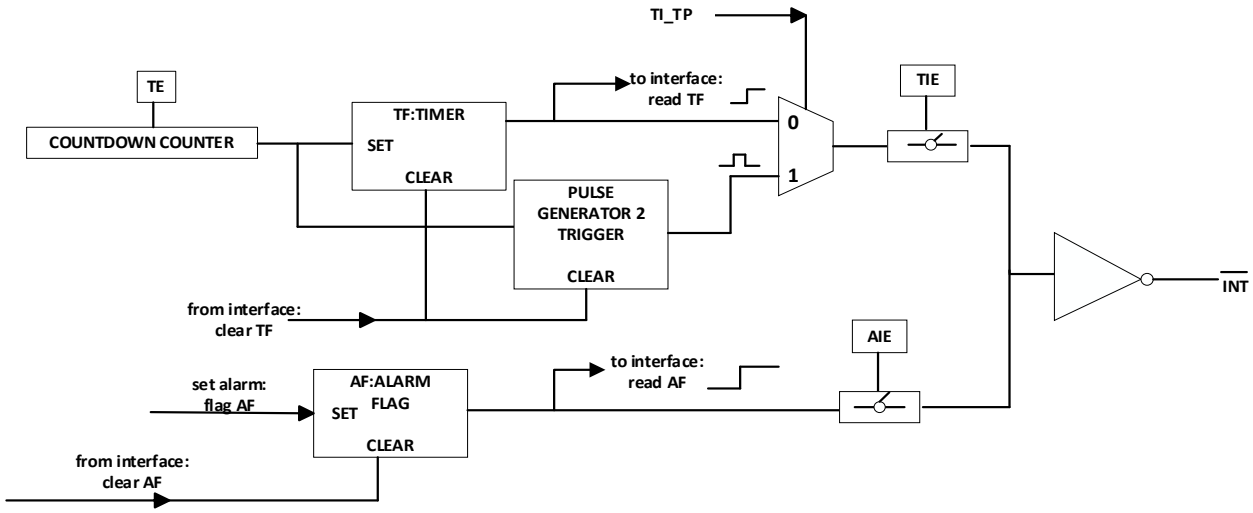



**Figure 3. Interrupt scheme**

**Bits TF and AF**: When an alarm occurs, AF is set to logic 1. Similarly, at the end of a timer countdown, TF is set to logic 1. These bits maintain their value until overwritten using the interface. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.

**Bits TIE and AIE:** These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

**Countdown timer interrupts:** The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies.

**Table 5. $\overline{\text{INT}}$ operation (bit TI_TP = 1)[1]**

| SOURCE CLOCK (Hz) | $\overline{\text{INT}}$ PERIOD (s) | |
|---|---|---|
| | n = 1[2] | n > 1[2] |
| 4096 | 1/8192 | 1/4096 |
| 64 | 1/128 | 1/64 |
| 1 | 1/64 | 1/64 |
| 1/60 | 1/64 | 1/64 |

[1] TF and $\overline{\text{INT}}$ become active simultaneously.

[2] n = loaded countdown value. Timer stops when n = 0.

## 6.4 Time and Date Registers

The majority of the registers are coded in the BCD format to simplify application use.

### 6.4.1 Register VL_seconds

**Table 6. VL_seconds - seconds and clock integrity status register (address 02h) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 | VL | 0 | - | clock integrity is guaranteed |
| | | 1 (Start-up value) | - | integrity of the clock information is not guaranteed |
| 6 to 4 | SECONDS | 0 to 5 | ten's place | actual seconds coded in BCD format, see Table 7 |
| 3 to 0 | | 0 to 9 | unit place | |

**Table 7. Seconds coded in BCD format**

| SECONDS VALUE (decimal) | UPPER-DIGIT (ten's place) | | | DIGIT (unit place) | | | |
|---|---|---|---|---|---|---|---|
| | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 02 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| : | : | : | : | : | : | : | : |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| : | : | : | : | : | : | : | : |
| 58 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 59 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

#### 6.4.1.1 Voltage-low Detector and Clock Monitor

The GX8563 has an on-chip voltage-low detector (see Figure 4). When $V_{DD}$ drops below $V_{low}$, bit VL in the VL_seconds register is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by using the interface.

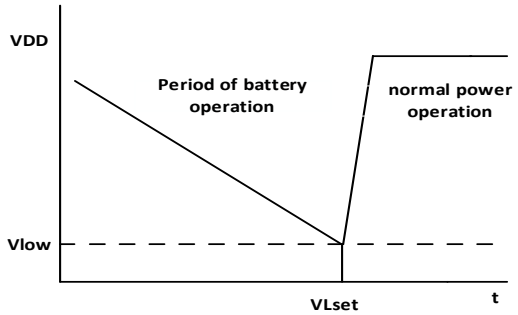



**Figure 4. Voltage-low detection**

The VL flag is intended to detect the situation when VDD is decreasing slowly, for example under battery operation. Should the oscillator stop or VDD reach Vlow before power is re-asserted, then the VL flag is set. This will indicate that the time may be corrupted.

### 6.4.2 Register Minutes

**Table 8. Minutes - minutes register (address 03h) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 | - | - | - | unused |
| 6 to 4 | MINUTES | 0 to 5 | ten's place | actual minutes coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 6.4.3 Register Hours

**Table 9. Hours - hours register (address 04h) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 to 6 | - | - | - | unused |
| 5 to 4 | HOURS | 0 to 2 | ten's place | actual hours coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 6.4.4 Register Days

**Table 10. Days - days register (address 05h) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 to 6 | - | - | - | unused |
| 5 to 4 | DAYS[1] | 0 to 3 | ten's place | actual day coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

[1] The GX8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

### 6.4.5 Register Weekdays

**Table 11. Weekdays - weekdays register (address 06h) bit description**

| BIT | SYMBOL | VALUE | DESCRIPTION |
|---|---|---|---|
| 7 to 3 | - | - | unused |
| 2 to 0 | WEEKDAYS | 0 to 6 | actual weekday values, see Table 12 |

**Table 12. Weekday assignments**

| DAY[1] | BIT | | |
|---|---|---|---|
| | 2 | 1 | 0 |
| Sunday | 0 | 0 | 0 |
| Monday | 0 | 0 | 1 |
| Tuesday | 0 | 1 | 0 |
| Wednesday | 0 | 1 | 1 |
| Thursday | 1 | 0 | 0 |
| Friday | 1 | 0 | 1 |
| Saturday | 1 | 1 | 0 |

[1] Definition may be re-assigned by the user.

### 6.4.6 Register Century_months

**Table 13. Century_months - century flag and months register (address 07h) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 | C[1] | 0[2] | - | indicates the century is x |
| | | 1 | - | indicates the century is x+1 |
| 6 to 5 | - | - | - | unused |
| 4 | MONTHS | 0 to 1 | ten's place | actual month coded in BCD format, see Table 14 |
| 3 to 0 | | 0 to 9 | unit place | |

[1] This bit may be re-assigned by the user.

[2] This bit is toggled when the register Years overflows from 99 to 00.

**Table 14. Month assignments in BCD format**

| MONTH | UPPER-DIGIT (ten's place) | DIGIT (unit place) | | | |
|---|---|---|---|---|---|
| | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| January | 0 | 0 | 0 | 0 | 1 |
| February | 0 | 0 | 0 | 1 | 0 |
| March | 0 | 0 | 0 | 1 | 1 |
| April | 0 | 0 | 1 | 0 | 0 |
| May | 0 | 0 | 1 | 0 | 1 |
| June | 0 | 0 | 1 | 1 | 0 |
| July | 0 | 0 | 1 | 1 | 1 |
| August | 0 | 1 | 0 | 0 | 0 |
| September | 0 | 1 | 0 | 0 | 1 |
| October | 1 | 0 | 0 | 0 | 0 |
| November | 1 | 0 | 0 | 0 | 1 |
| December | 1 | 0 | 0 | 1 | 0 |

### 6.4.7 Register Years

**Table 15. Years - years register (08h) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 to 4 | YEARS | 0 to 9 | ten's place | actual year coded in BCD format[1] |
| 3 to 0 | | 0 to 9 | unit place | |

[1] When the register Years overflows from 99 to 00, the century bit C in the register Century_months is toggled.

## 6.5 Setting and Reading The Time

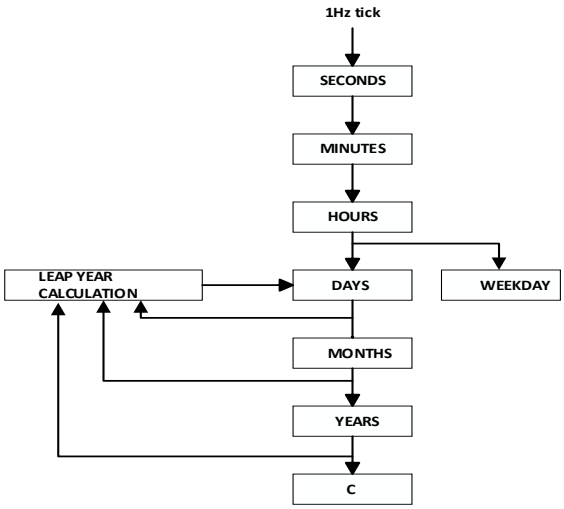



**Figure 5. Data flow for the time function**

Shows the data flow and data dependencies starting from the 1 Hz clock tick.

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents faulty reading of the clock and calendar during a carry condition and incrementing the time registers, during the read cycle.

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second.

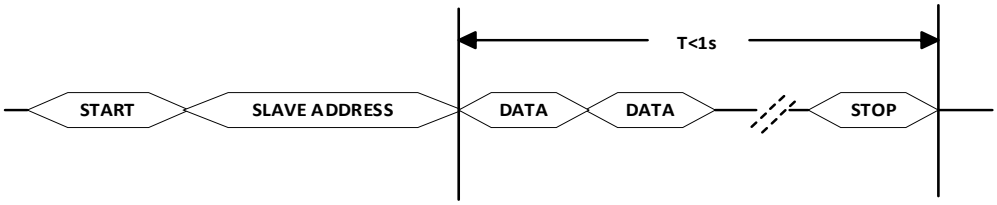



**Figure 6. Access time for read/write operations**

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or

reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address for write (A2h).
2. Set the address pointer to 2 (VL_seconds) by sending 02h.
3. Send a RESTART condition or STOP followed by START.
4. Send the slave address for read (A3h).
5. Read VL_seconds.
6. Read Minutes.
7. Read Hours.
8. Read Days.
9. Read Weekdays.
10. Read Century_months.
11. Read Years.
12. Send a STOP condition.

## 6.6 Alarm Registers

### 6.6.1 Register Minute_alarm

**Table 16. Minute_alarm - minute alarm register (address 09h) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 | AE_M | 0 | - | minute alarm is enabled |
| | | default 1 | - | minute alarm is disabled |
| 6 to 4 | MINUTE_ALARM | 0 to 5 | ten's place | minute alarm information coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 6.6.2 Register Hour_alarm

**Table 17. Hour_alarm - hour alarm register (address 0Ah) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 | AE_H | 0 | - | hour alarm is enabled |
| | | default 1 | - | hour alarm is disabled |
| 6 | - | - | - | unused |
| 5 to 4 | HOUR_ALARM | 0 to 2 | ten's place | hour alarm information coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 6.6.3 Register Day_alarm

**Table 18. Day_alarm - day alarm register (address 0Bh) bit description**

| BIT | SYMBOL | VALUE | PLACE VALUE | DESCRIPTION |
|---|---|---|---|---|
| 7 | AE_D | 0 | - | day alarm is enabled |
| | | default 1 | - | day alarm is disabled |
| 6 | - | - | - | unused |
| 5 to 4 | DAY_ALARM | 0 to 3 | ten's place | day alarm information coded in BCD format |
| 3 to 0 | | 0 to 9 | unit place | |

### 6.6.4 Register Weekday_alarm

**Table 19. Weekday_alarm - weekday alarm register (address 0Ch) bit description**

| BIT | SYMBOL | VALUE | DESCRIPTION |
|---|---|---|---|
| 7 | AE_W | 0 | weekday alarm is enabled |
| | | default 1 | weekday alarm is disabled |
| 6 to 3 | - | - | unused |
| 2 to 0 | WEEKDAY_ALARM | 0 to 6 | weekday alarm information coded in BCD format |

### 6.6.5 Alarm Flag

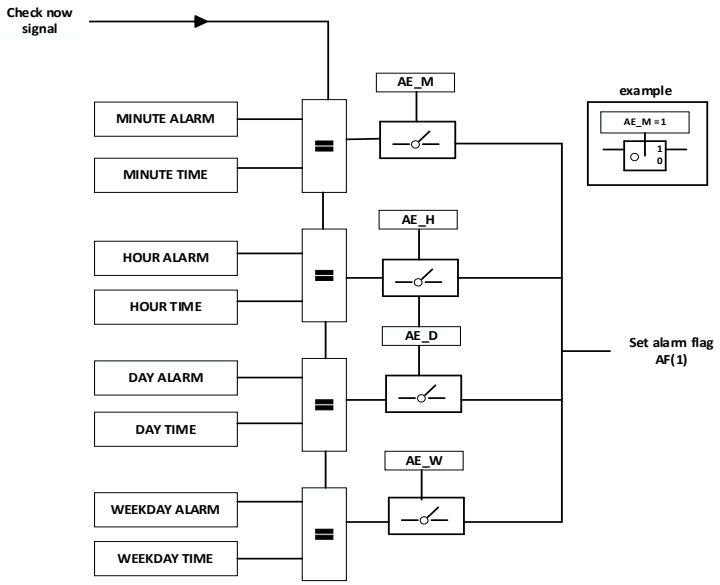



**Figure 7. Alarm function block diagram**

Only when all enabled alarm settings are matching. It's only on increment to a matched case that the alarm flag is set.

By clearing the alarm enable bit (AE_x) of one or more of the alarm registers, the corresponding alarm condition(s) are active. When an alarm occurs, AF is set to logic 1. The asserted AF can be used to generate an interrupt (INT). The AF is cleared using the interface.

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day or weekday, and its corresponding AE_x is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the alarm flag (AF in register Control_2) is set to logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF will remain set until cleared by the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_x bit at logic 1 are ignored.

## 6.7 Register CLKOUT_control and Clock Output

Frequencies of 32.768 kHz (default), 1.024 kHz, 32 Hz, and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

**Table 20. CLKOUT_control - CLKOUT control register (address 0Dh) bit description**

| BIT | SYMBOL | VALUE | DESCRIPTION |
|---|---|---|---|
| 7 | FE | 0 | the CLKOUT output is inhibited and CLKOUT output is set high-impedance |
| | | default 1 | the CLKOUT output is activated |
| 6 to 2 | - | - | unused |
| 1 to 0 | FD[1:0] | | frequency output at pin CLKOUT |
| | | 00 | 32.768kHz |
| | | 01 | 1.024kHz |
| | | 10 | 32Hz |
| | | 11 | 1Hz |

## 6.8 Timer Function

The 8-bit countdown timer at address 0Fh is controlled by the Timer_control register at address 0Eh. The Timer_control register determines one of 4 source clock frequencies for the timer (4.096 Hz, 64 Hz, 1 Hz, or 1⁄60 Hz), and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The TF may only be cleared by using the interface. The asserted TF can be used to generate an interrupt on pin INT. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the state of TF. Bit TI_TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

### 6.8.1 Register Timer_control

**Table 21. Timer_control - timer control register (address 0Eh) bit description**

| BIT | SYMBOL | VALUE | DESCRIPTION |
|---|---|---|---|
| 7 | TE | 0[1] | timer is disabled |
| | | 1 | timer is enabled |
| 6 to 2 | - | - | unused |
| 1 to 0 | TD[1:0] | | timer source clock frequency select[2] |
| | | 00 | 4.096kHz |
| | | 01 | 64Hz |
| | | 10 | 1Hz |
| | | 11[2] | 1/60Hz |

[1] Default value.

[2] These bits determine the source clock for the countdown timer; when not in use, TD[1:0] should be set to 1⁄60 Hz for power saving.

### 6.8.2 Register Timer

**Table 22. Timer - timer value register (address 0Fh) bit description**

| BIT | SYMBOL | VALUE | DESCRIPTION |
|---|---|---|---|
| 7 to 0 | TIMER[7:0] | 00h to FFh | countdown period in seconds: $\text{CountdownPeriod} = \frac{n}{SourceClockFrequency}$ |
| where n is the countdown value | | | |

**Table 23. Timer register bits value range**

| BIT | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

The register Timer is an 8-bit binary countdown timer. It is enabled and disabled via the Timer_control register bit TE. The source clock for the timer is also selected by the Timer_control register. Other timer properties such as interrupt generation are controlled via the register Control_status_2.

For accurate read back of the count down value, it is recommended to read the register twice and check for consistent results, since it is not possible to freeze the countdown timer counter during read back.

## 6.9 EXT_CLK Test Mode

A test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in register Control_status_1. Then pin CLKOUT becomes an input. The test mode replaces the internal 64 Hz signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT will then generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1 000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 26 divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0 (STOP must be cleared before the prescaler can operate again).

Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

### 6.9.1 Operation Example:

1. Set EXT_CLK test mode (Control_status_1, bit TEST1 = 1).
2. Set STOP (Control_status_1, bit STOP = 1).
3. Clear STOP (Control_status_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 64 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

## 6.10 STOP Bit Function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler ($F_3$ to $F_{14}$) to be held in reset and thus no 1 Hz ticks will be generated (see Figure 8). The time circuits can then be set and will not increment until the STOP bit is released (see Figure 9).

The STOP bit function will not affect the output of 32.768 kHz on CLKOUT, but will stop the generation of 1.024 kHz, 32 Hz, and 1 Hz.

The lower three stages of the prescaler ($F_0$ and $F_1$ and $F_3$) are not reset; and because the $I^2C$-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between zero and one 4096 Hz cycle (see Figure 9).

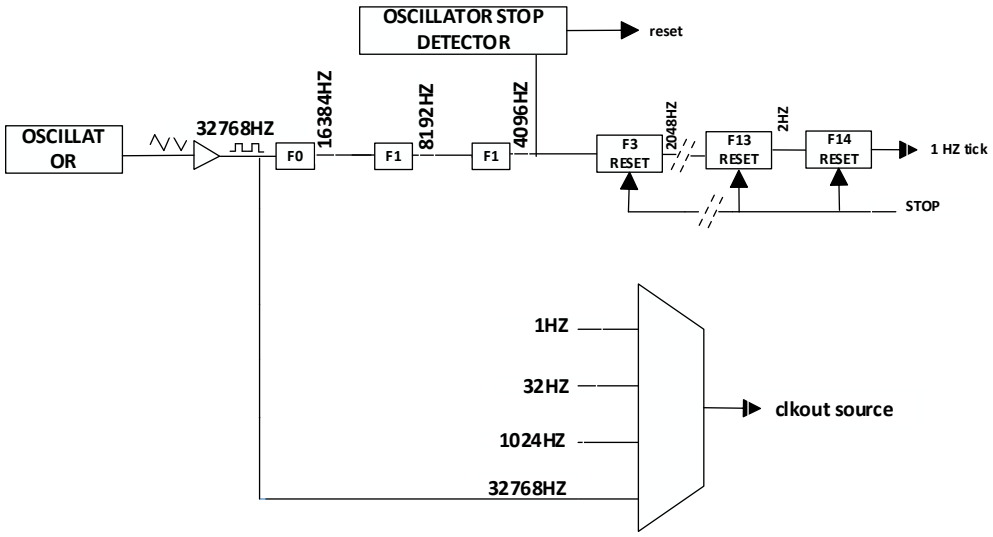



**Figure 8. STOP bit functional diagram**

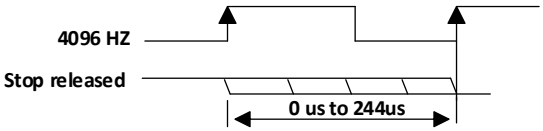



**Figure 9. STOP bit release timing**

## 6.11 Reset

The GX8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I²C-bus logic is initialized including the address pointer and all registers are set according to Table 25. I²C-bus communication is not possible during reset.

**Table 25. Register reset value[1]**

| ADDRESS | REGISTER NAME | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00h | Control_status_1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 01h | Control_status_2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | VL_seconds | 1 | x | x | x | x | x | x | x |
| 03h | Minutes | x | x | x | x | x | x | x | x |
| 04h | Hours | x | x | x | x | x | x | x | x |
| 05h | Days | x | x | x | x | x | x | x | x |
| 06h | Weekdays | x | x | x | x | x | x | x | x |
| 07h | Century_months | x | x | x | x | x | x | x | x |
| 08h | Years | x | x | x | x | x | x | x | x |
| 09h | Minute_alarm | 1 | x | x | x | x | x | x | x |
| 0Ah | Hour_alarm | 1 | x | x | x | x | x | x | x |
| 0Bh | Day_alarm | 1 | x | x | x | x | x | x | x |
| 0Ch | Weekday_alarm | 1 | x | x | x | x | x | x | x |
| 0Dh | CLKOUT_control | 1 | x | x | x | x | x | 0 | 0 |
| 0Eh | Timer_control | 0 | x | x | x | x | x | 1 | 1 |
| 0Fh | Timer | x | x | x | x | x | x | x | x |

[1] Registers marked x are undefined at power-up and unchanged by subsequent resets.

# 7 Characteristics of The I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

## 7.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 11).

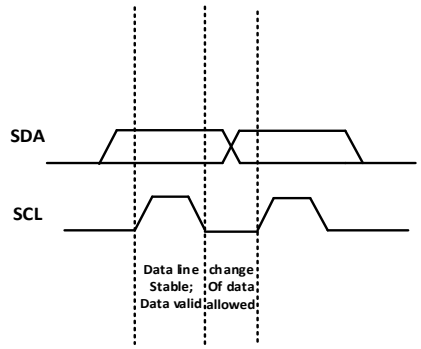



**Figure 11. Bit transfer**

## 7.2 START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 12).

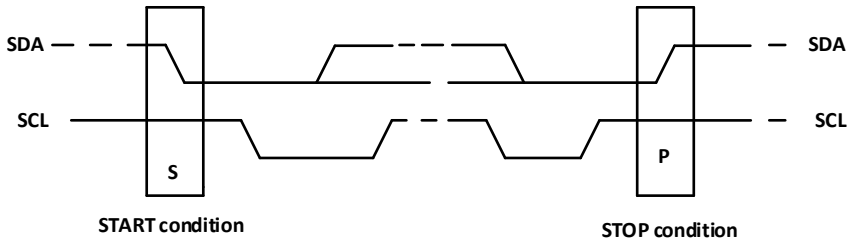



**Figure 12. Definition of START and STOP conditions**

## 7.3 System Configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see Figure 13).

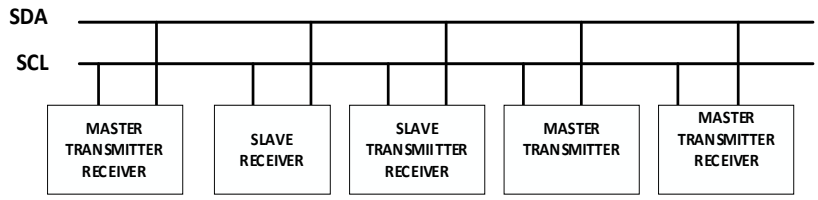



**Figure 13. System configuration**

## 7.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

• A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.

• Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

• The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

• A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I2C-bus is illustrated in Figure 14.

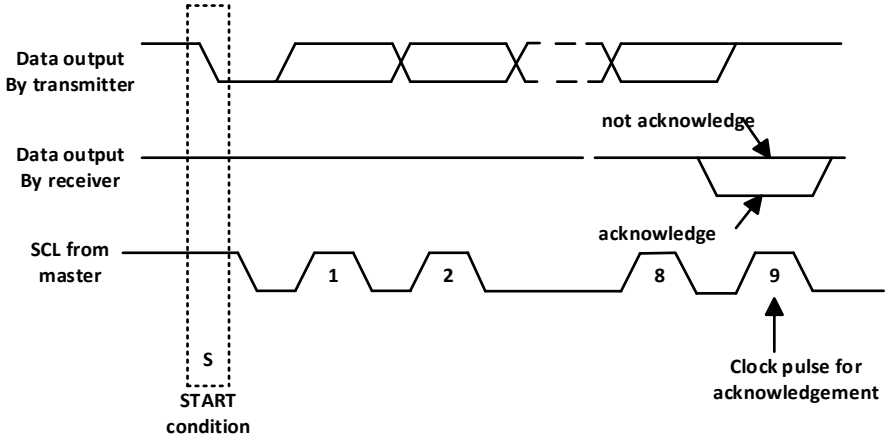



**Figure 14. Acknowledgement on the $I^2C$-bus**

## 7.5 I²C-bus Protocol

### 7.5.1 Addressing

Before any data is transmitted on the I2C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The GX8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

Two slave addresses are reserved for the GX8563:

Read: A3h (10100011)

Write: A2h (10100010)

The GX8563 slave address is illustrated in Figure 15.

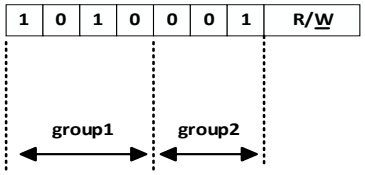



**Figure 15. Slave address**

### 7.5.2 Clock and Calendar READ or WRITE Cycles

The I²C-bus configuration for the different GX8563 READ and WRITE cycles is shown in Figure 16, Figure 17 and Figure 18. The register address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the register address are not used.

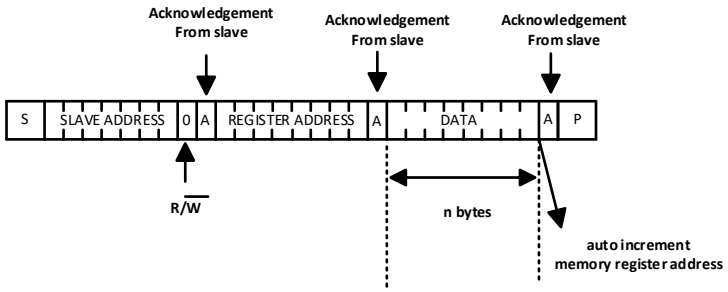



**Figure 16. Master transmits to slave receiver (WRITE mode)**

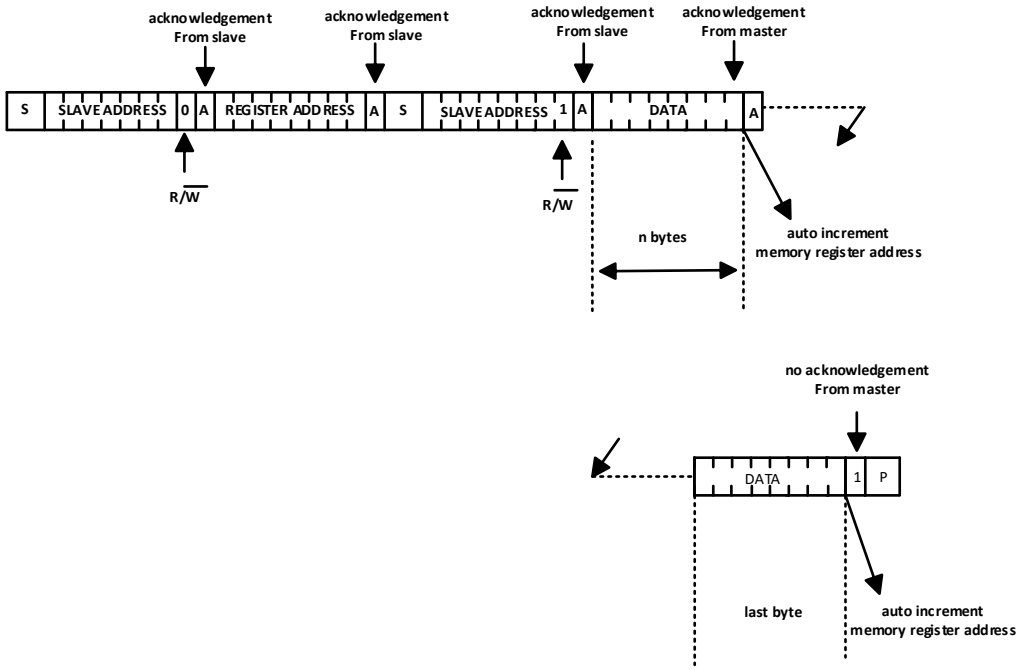



**Figure 17. Master reads after setting register address (write register address; READ data)**

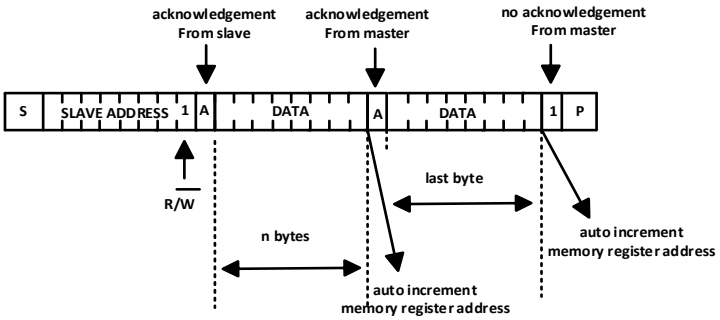



**Figure 18. Master reads slave immediately after first byte (READ mode)**

## 8 Internal Circuitry

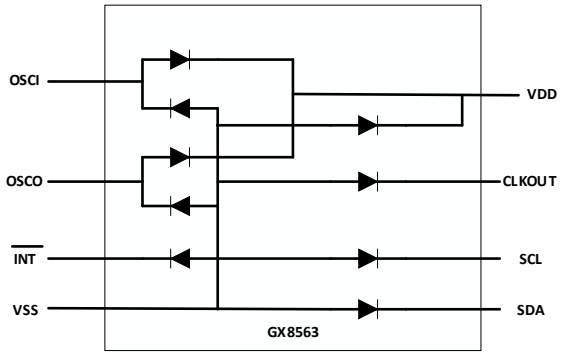



**Figure 20. Device diode protection diagram**

## 9 Limiting Values

**Table 26. Limiting values**

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | -0.5 | +6.5 | V |
| $I_{DD}$ | supply current | | +50 | +50 | mA |
| $V_I$ | input voltage | on pins SCL, SDA, and OSCI | -0.5 | +6.5 | V |
| $V_O$ | output voltage | on pins CLKOUT and INT | -0.5 | +6.5 | V |
| $I_I$ | input current | at any input | -10 | +10 | mA |
| IO | output current | at any output | -10 | +10 | mA |
| Ptot | total power dissipation | | - | 300 | mW |
| $V_{ESD}$ | electrostatic discharge voltage | HBM（MSOP8） | - | ±8000 | V |
| $T_{stg}$ | storage temperature | | -65 | +150 | ℃ |
| $T_{amb}$ | ambient temperature | operating device | -40 | +85 | ℃ |

## 10 Static Characteristics

**Table 27. Static characteristics**

$V_{DD}$ = 1.0 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ =-40°C to +85°C; $f_{osc}$ = 32.768 kHz; quartz $R_s$ = 30 kΩ; $C_L$ = 8 pF;

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DD}$ | supply voltage | interface inactive; fSCL = 0 Hz; $T_{amb}$ = 25°C[1] | 1.0 | - | 5.5 | V |
| | | interface active; $f_{SCL}$ = 400 kHz[1] | 1.8 | - | 5.5 | V |
| | | clock data integrity; $T_{amb}$ = 25°C | $V_{low}$ | - | 5.5 | V |
| $I_{DD}$ | supply current | interface active | | | | |
| | | $f_{SCL}$ = 400 kHz | - | - | 800 | µA |
| | | $f_{SCL}$ = 100 kHz | - | - | 200 | µA |
| | | interface inactive ($f_{SCL}$=0Hz); CLKOUT disabled; $T_{amb}$ = 25°C[2] | | | | |
| | | VDD = 5.0 V | - | 400 | 600 | nA |
| | | VDD = 3.0 V | - | 250 | 500 | nA |
| | | interface inactive ($f_{SCL}$=0 Hz); CLKOUT disabled; $T_{amb}$= -40°C to +85°C[2] | | | | |
| | | VDD = 5.0 V | - | 500 | 700 | nA |
| | | VDD = 3.0 V | - | 400 | 600 | nA |
| **Inputs** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | $V_{SS}$ | - | 0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD}$ | - | $V_{DD}$ | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | -1 | 0 | +1 | uA |
| $C_i$ | input capacitance | | - | - | 7 | pF |
| **Outputs** | | | | | | |
| $I_{OL}$ | LOW-level output current | output sink current; $V_{OL}$ = 0.4 V; $V_{DD}$ = 5 V | | | | |
| | | on pin SDA | 3 | - | - | mA |
| | | on pin INT | 1 | - | - | mA |
| | | on pin CLKOUT | 1 | - | - | mA |
| $I_{LO}$ | output leakage current | $V_O$ = $V_{DD}$ or $V_{SS}$ | -1 | 0 | +1 | uA |
| **Voltage detector** | | | | | | |
| $V_{low}$ | low voltage | $T_{amb}$ = 25°C; sets bit VL; | - | 0.9 | 1.0 | V |

[1] For reliable oscillator start-up at power-up: $VDD_{(min)power-up}$ = $V_{DD(min)}$ + 0.3 V.

[2] Timer source clock = 1/60 Hz, level of pins SCL and SDA is $V_{DD}$ or $V_{SS}$.

## 11 Dynamic Characteristics

**Table 28. Dynamic characteristics**

$V_{DD}$ = 1.0 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ =-40°C to +85°C; $f_{osc}$ = 32.768 kHz; quartz $R_s$ = 30 kΩ;

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Quartz crystal parameters (f = 32.768 kHz)** | | | | | | |
| $R_S$ | series resistance | | - | 30 | 40 | kΩ |
| $C_L$ | load capacitance | external; on pin OSCI OSCO | 5 | 12 | 20 | pF |
| | | | | | | |
| **CLKOUT output** | | | | | | |
| $\delta_{CLKOUT}$ | duty cycle on pin CLKOUT | | - | 50 | - | % |
| **I²C-bus timing characteristics** | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | - | - | 400 | kHz |
| $t_{HD;STA}$ | hold time (repeated) START condition | | 0.6 | - | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 0.6 | - | - | µs |
| $t_{LOW}$ | LOW period of the SCL clock | | 1.3 | - | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | 0.6 | - | - | µs |
| $t_r$ | rise time of both SDA and SCL signals | | | | | |
| | | standard-mode | - | - | 1 | µs |
| | | fast-mode | - | - | 0.3 | µs |
| $t_f$ | fall time of both SDA and SCL signals | | - | - | 0.3 | µs |
| $t_{BUF}$ | bus free time between a STOP and START condition | | 1.3 | - | - | µs |
| $C_b$ | capacitive load for each bus line | | - | - | 400 | pF |
| $t_{SU;DAT}$ | data set-up time | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | - | - | ns |
| $t_{SU;STO}$ | set-up time for STOP condition | | 0.6 | - | - | µs |
| $t_{w(spike)}$ | spike pulse width | on bus | - | - | 50 | ns |

[1] $C_L$ are the two parallel cap connected to the crystal, should be adjusted with different crystal

[2] Unspecified for $f_{CLKOUT}$ = 32.768 kHz.

[3] All timing values are valid within the operating supply voltage at ambient temperature and referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.

[4] I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

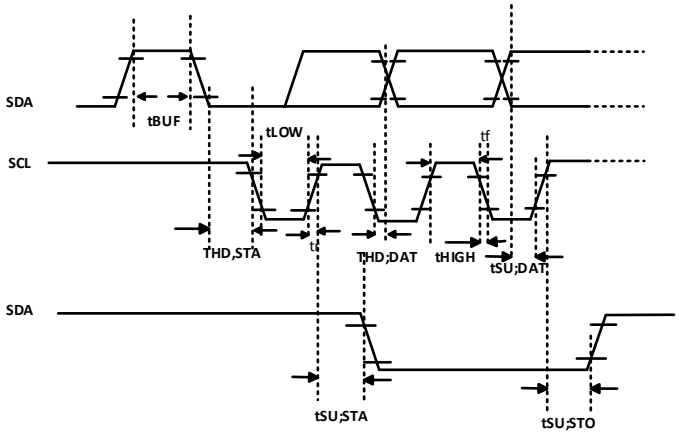



Figure 21. I²C-bus timing waveforms

## 12 Situation of application

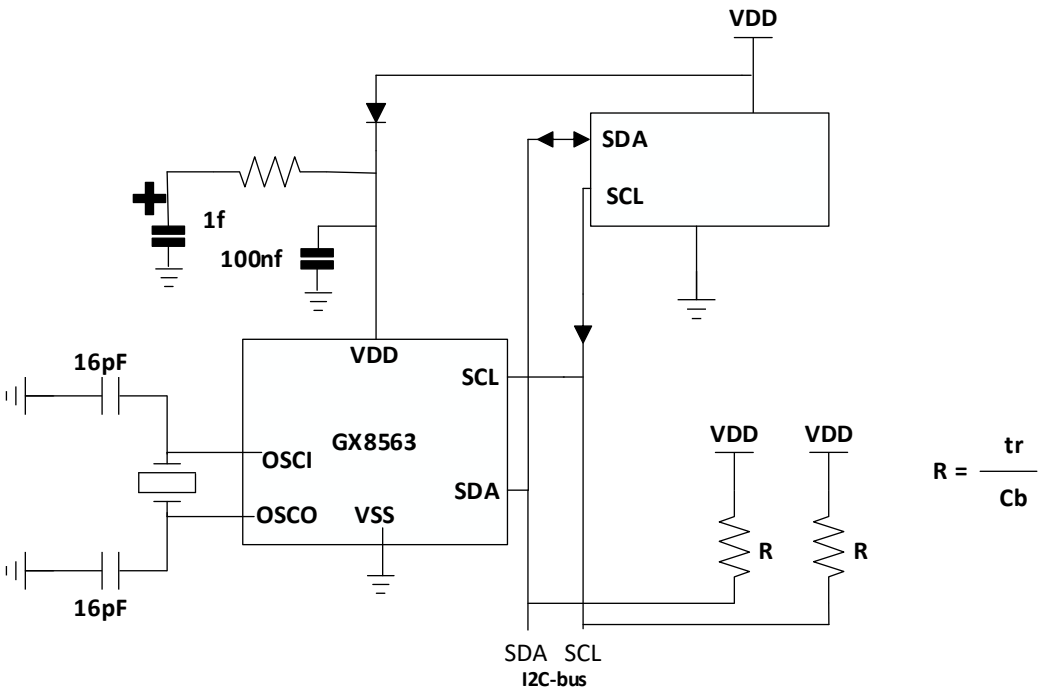
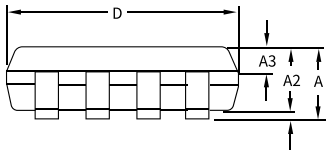
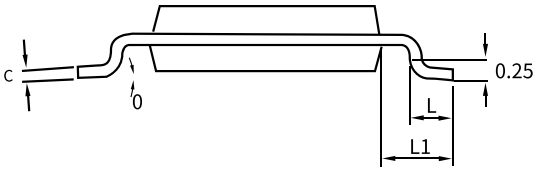


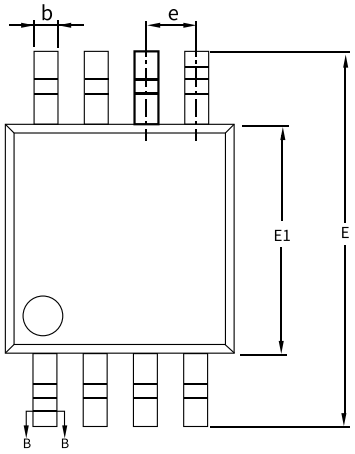

Figure 22. Application diagram

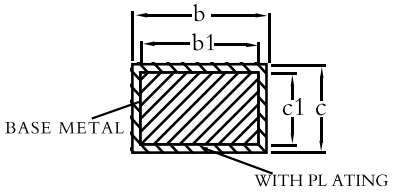
## 13 Package Outline

MSOP8 MSL3



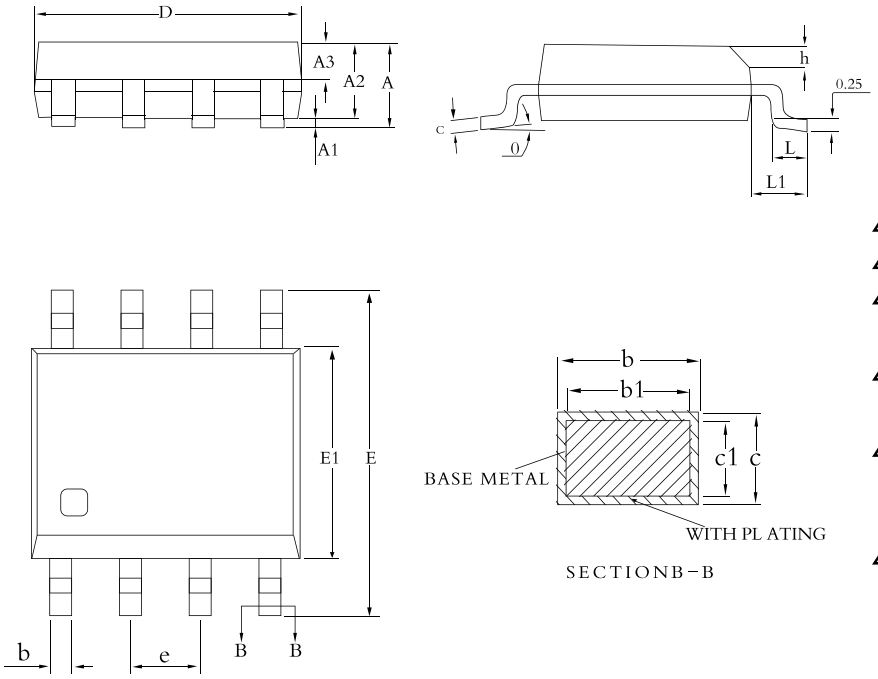




SECTIONB-B

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.10 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| A3 | 0.30 | 0.35 | 0.40 |
| b | 0.28 | — | 0.36 |
| b1 | 0.27 | 0.30 | 0.33 |
| c | 0.15 | — | 0.19 |
| c1 | 0.14 | 0.15 | 0.16 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.70 | 4.90 | 5.10 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 0.65BSC | | |
| L | 0.40 | — | 0.70 |
| L1 | 0.95REF | | |
| θ | 0 | — | 8° |

SOP8 MSL3




| | SYMBOL | MILLIMETER | | |
|---|---|---|---|---|
| | | MIN | NOM | MAX |
| | A | ___ | ___ | 1.75 |
| | A1 | 0.10 | ___ | 0.225 |
| | A2 | 1.30 | 1.40 | 1.50 |
| | A3 | 0.60 | 0.65 | 0.70 |
| 1 | b | 0.39 | ___ | 0.47 |
| 1 | b1 | 0.38 | 0.41 | 0.44 |
| 1 | c | 0.20 | ___ | 0.24 |
| | c1 | 0.19 | 0.20 | 0.21 |
| 1 | D | 4.80 | 4.90 | 5.00 |
| | E | 5.80 | 6.00 | 6.20 |
| 1 | E1 | 3.80 | 3.90 | 4.00 |
| | e | 1.27BSC | | |
| | h | 0.25 | ___ | 0.50 |
| 1 | L | 0.50 | ___ | 0.80 |
| | L1 | 1.05REF | | |
| | 0 | 0 | ___ | 8° |

# 14 Ordering Information

**Table 29. Ordering information**

| Purchase Number | Device | PIN-Package | SPQ | Remarks |
|---|---|---|---|---|
| GX8563U-T&R | GX8563U | MSOP8 | 4000 | Tape & Reel |
| GX8563Z-T&R | GX8563Z | SOP8 | 4000 | Tape & Reel |